AMENDMENT OF THE SPECIFICATION

In response to the objection for paragraph [0009] of item 2, Applicant respectfully requests that the following amended paragraph replace paragraph [0009] (lines 20-28 on p. 3, lines 1 & 2 on p. 4) of the application specification in the "Object of the Invention" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> The accomplishment of these and other related objects is achieved by a method of ~~shortening a single-bit error correction/ double-bit error detection code for~~ detecting and correcting random bit errors in a digital transmission system using a shortened single-bit error correction/double-bit error detection code wherein data is scrambled after said error detection/correction code is applied over a set of data and wherein said set of data is subsequently checked, after descrambling, for detecting and correcting transmission errors, to still obtain unique syndromes for said random bit errors after they have been multiplied as a result of said descrambling, said method of ~~shortening~~ detecting and correcting random bit errors including:

In response to the objection for paragraph [0021] of item 2, Applicant respectfully requests that the following amended paragraph replace paragraph [0021] (lines 2 & 3 on p. 5) of the specification in the "Object of the Invention" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> wherein said predetermined forward error correction code is determined ~~as described above.~~ via a shortened single-bit error correction/double-bit error detection code.

In response to the objection for paragraph [0060] of item 2, Applicant respectfully requests that the following amended paragraph replace paragraph [0060] (lines 14-29 on p. 12) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> A common data unit often manipulated by modern data communications devices, such as switches and routers, is a 64-byte or 512-bit data packet thus requiring eight 64B/66B !blocks of the kind shown in figure 1 (120). FEC applied at packet level i.e., over eight 8-byte or 64-bit blocks (300), requires 11 bits as this is discussed in detail in the following description of the invention. Hence, in this case, overhead becomes (8x2 + 11) / (512-11) or 5.4% which is a modest increase over the original 3% overhead of the 64B/66B while permitting single-bit transmission error corrections. Since, in practice, more than ~~a weird~~ an odd-sized 11-bit field would likely have to be reserved in a 512-bit payload a maximum of 6.4% may have to be considered if a 2-byte field would be reserved for practical considerations. Hence, FEC requires that redundant bits be taken from the payload under the form of a FCS (field check sequence) generally placed at the end of the packet (310).

In response to the objection for paragraphs [0067] and [0068], under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0067] (lines 19-32 on p. 13, lines 1-7 on p. 14) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> Before discussing how the forward error may be generated, ~~It~~ it is worth noting here that figure 3 shows blocks and packet in a traditional way i.e., with block preamble and beginning of packet (BOP) shown on the left. The most left bit is considered as the most significant bit and is transmitted first thus, from left

to right, so as FCS is transmitted last with the end of packet (EoP). However, this is not consistent with the representation of the scrambler and descrambler by the standard as shown in figure 2. By referring to this figure one can notice that MSB, i.e. 2^{58}, is shown to be the most right bit of the shift register. By referring to the proper literature on the subject for example: 'Error-Correcting Codes', Peterson & Weldon, 2nd edition, The MIT press, 1972, and more specifically to chapter 7 'Linear Switching Circuit' it can easily be found that scrambler and de-scrambler of the 10GbE standard are rather implementing the reciprocal of the scrambling polynomial quoted above; i.e. ~~G(x)~~ $G_s(x) = X^{58} + X^{19} + 1$ and scrambler and de-scrambler should rather be indexed from 58 to 0, from left to right (so as the middle term is 2^{19}). This does not change anything in practice both polynomials have exactly the same properties however, ~~the invention needs~~ one may need to consider the right indexing to ~~be understood~~ understand the described embodiments and the forward error correction codes.

Also in response to the objection for paragraphs [0067] and [0068], under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0068] (lines 8-10) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

Hence, the rest of the description assumes that the scrambling polynomial is actually ~~G(x)~~ $G_s(x) = X^{58} + X^{19} + 1$ with, as usual, the most significant term on the left.

Also in response to the objection for paragraphs [0067] and [0068], under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0049] (lines 3-6 on p. 9) of the specification in the "Detailed Description of the Preferred Embodiment" section.

Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> Figure 2 shows the conventional representation of the l0GbE scrambler and descrambler i.e., implementing, according to the standard (see however the remark at the end of figure 3), the polynomial: ~~G(x)~~ $\underline{G_s(x)} = 1 + X^{19} + X^{58}$

Also in response to the objection for paragraphs [0067] and [0068], under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0050] (lines 7-19 on p. 9) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

> Scrambler (200) and descrambler (210) are linear feedback shift register (LFSR) to perform respectively, continuous division and multiplication of binary strings i.e., in an algebra modulo 2 modulo ~~G(x)~~ $\underline{G_s(x)}$, one bit at a time. Adders are XOR's such as (205). The two 58-bit shift registers have taps at indexes 0, 39 and 58 corresponding to the powers of the three terms of ~~G(x)~~ $\underline{G_s(x)}$, a primitive irreducible polynomial thus capable of generating a pseudo-random maximum length sequence. Sequence will repeat only after 2^{58}-1 shifts i.e., never for all practical purposes since, even though there would be one shift possible every 1 pico (10^{-12}) second, the time to wrap around the sequence would still be larger than the time that has elapsed since the creation of the universe.

Also in response to the objection for paragraphs [0067] and [0068], under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0052] (lines 5-15 on p. 10) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

However, an undesirable well-known effect of scrambling is illustrated with the second example of an all-zero pattern (230) to transmit. This, after scrambling, thus gives pattern (231) in which an error is assumed to flip 5th bit from left (233), when signal is propagated through the transmission medium. Then, after descrambling, not only 5th bit is false but two more errors are created (237, 239) in the restored pattern (232). The three errors are spread at distances corresponding to the powers of ~~G(x)~~ $G_s(x)$ terms. Indeed, scrambling multiplies the errors by a number corresponding to the number of terms of the scrambling polynomial in use i.e., 3 with l0GbE polynomial.

Also in response to the objection for paragraphs [0067], [0068], and [0071] under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0071] (lines 20-27 on p. 14) of the specification in the "Detailed Description of the Preferred Embodiment" section. Deletions are shown by strikethrough while added matter changes are shown with underlining. The changes to this paragraph do not add new matter:

First, all shifts of three-bit errors (410) spaced as ~~G(x)~~ $G_s(x)$ i.e., at indexes 58, 19 and 0 and entirely contained in the packet payload (including FCS), must have unique syndrome values once packet is FEC checked so that they can be unambiguously corrected. These errors are of the kind shown in figure 3 (320). When this happens no single-bit error or double-bit error respectively of the type (330) and (340) shown in figure 3 ~~may have possibly~~ is assumed to have occurred in previous packet.

In response to the objection for paragraph [0086] under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0086] (lines 1 & 2 on p. 18) of the specification in the "Detailed Description of the Preferred Embodiment" section. The changes to this paragraph do not add new matter:

For ~~a~~ the sake ~~a~~ of readability 0's are replaced by a dot (.) in the binary vectors shown.

In response to the objection for paragraph [0090] under item 2, Applicant respectfully requests that the following paragraph replace paragraph [0090] (lines 13-24 on p. 19) of the specification in the "Detailed Description of the Preferred Embodiment" section. The changes to this paragraph do not add new matter:

The above requires that code generated with suggested polynomial G(x) = (X+l) ($X^{10} + X^9 + X^7 + X^6 + X^4 + X^l + 1$) be shortened so combinations of three errors cannot return a vector greater than α^{1022} for the reason that next value would be α^0 (since group is a finite cyclic group). Indeed, the EoP single-bit errors i.e., (350) in figure 3, need to be unique according to the invention. As they are using the 39 starting vectors (620) of the multiplicative group they cannot be used by the three-bit error combinations. This is obtained by excluding the use of group vectors (630) beyond α^{914} (the 915th vector of the group) i.e., the 857 three-bit error combinations + 58, the degree of the scrambler polynomial.